ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

Field-Effect Transistors Based on Silicon Nanowire Arrays: Effect of the Good and the Bad Silicon Nanowires

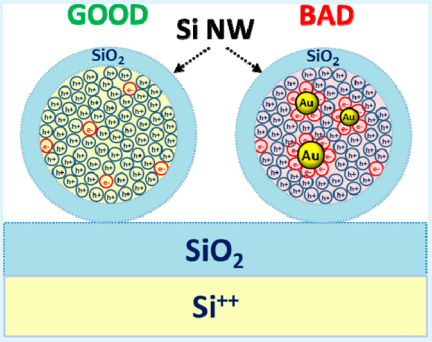
Bin Wang,[†] Thomas Stelzner,[‡] Rawi Dirawi,[†] Ossama Assad,[†] Nisreen Shehada,[†] Silke Christiansen,[§] and Hossam Haick*,[†]

[†]The Department of Chemical Engineering and the Russell Berrie Nanotechnology Institute, Technion − Israel Institute of Technology, Haifa 32000, Israel

[‡]Institute of Photonic Technology e.V., Albert-Einstein-Strasse 9, 07745 Jena, Germany

[§]Max-Planck-Institute for the Science of Light, Günther-Scharowsky-Strasse 1, 91058 Erlangen, Germany

ABSTRACT: Aligned arrays of silicon nanowires (*aa*-Si NWs) allow the exploitation of Si NWs in a scalable way. Previous studies explored the influence of the Si NWs' number, doping density, and diameter on the related electrical performance. Nevertheless, the origin of the observed effects still not fully understood. Here, we aim to provide an understanding on the effect of channel number on the fundamental parameters of *aa*-Si NW field effect transistors (FETs). Toward this end, we have fabricated and characterized 87 FET devices with varied number of Si NWs, which were grown by chemical vapor deposition with gold catalyst. The results show that FETs with Si NWs above a threshold number ($n > 80$) exhibit better device uniformity, but generally lower device performance, than FETs with lower number of Si NWs ($3 \leq n < 80$). Complementary analysis indicates that the obtained discrepancies could be explained by a weighted contribution of two main groups of Si NWs: (i) a group of gold-free Si NWs that exhibit high and uniform electrical characteristics; and (ii) a group of gold-doped Si NWs that exhibit inferior electrical characteristics. These findings are validated by a binomial model that consider the *aa*-Si NW FETs via a weighted combination of FETs of individual Si NWs. Overall, the obtained results suggest that the criterions used currently for evaluating the device performance (e.g., uniform diameter, length, and shape of Si NWs) do not necessarily guarantee uniform or satisfying electrical characteristics, raising the need for new growth processes and/or advanced sorting techniques of electrically homogeneous Si NWs.



KEYWORDS: *silicon nanowire, field effect transistor, array, scaling, gold, impurity*

INTRODUCTION

The ability of silicon nanowires (Si NWs) to carry electrical current makes them promising building blocks in various (opto)nanoelectronic and nanosensing devices.[1−10] For technological applications, the ease and effectiveness with which Si NWs are assembled and integrated into large-scale devices are significant, making the use of aligned arrays of Si NWs (*aa*-Si NWs) critically important.[11−22] Devices based on *aa*-Si NWs could (i) permit controllability over the sensitivity, response and recovery times, and device dimensions; (ii) bridge between the nanoscale and the macroscale worlds; and (iii) circumvent the requirement of position and structural control because the devices would display average properties of many distributed Si NWs.[11] Hence, the *aa*-Si NWs could be processed into devices of arbitrary size using conventional microfabrication technology.[11] Nevertheless, the low stability, reproducibility, and error tolerance still pose a challenge for realizing such devices for real-world technological applications. To overcome these challenges, it is essential to understand the scaling properties of *aa*-Si NWs.

Previous studies have explored the influence of Si NWs' number, doping density, and diameter in the context of nanowire electrical transport studies,[23,24] gas-phase chemical sensing,[5,25−27] and aqueous sensing of various species.[28−30] Nevertheless, the origin of the observed effects still not fully understood, mainly because of (i) the common assumption that Si NWs grown in a specific batch, under the same conditions, exhibit similar electrical characteristics to each other; (ii) the common assumption that Si NWs with similar diameter, length and/or shape exhibit similar electrical characteristics to each other; and (iii) the lack of correlation between the electrical and material properties of the Si NWs. In this study, we devised a fabrication process for field effect transistors (FETs) with a carefully controlled Si NWs' number between the source and drain electrodes. We study the effect of the number of Si NWs on the FET performance and provide a model that could help future designs of efficient and reproducible *aa*-Si NW FETs.

EXPERIMENTAL SECTION

Growth of the Si NWs. P-type Si NWs with an average diameter of 40 ± 8 nm and an average length of 8.5 ± 1.5 μm were grown on Si

Received: May 30, 2012
Accepted: July 20, 2012
Published: July 20, 2012

   dx.doi.org/10.1021/am300961d | *ACS Appl. Mater. Interfaces* 2012, 4, 4251−4258

wafers by chemical vapor deposition, using SiH_4 and B_2H_6 (1:20000 of B:Si ratio) as precursor gases and gold as a catalyst for the one-dimensional growth of Si NWs.[31]

Deposition and Imaging of the Si NW Arrays. The as-grown Si NWs were first etched in a buffered hydrofluoric acid for 15 s and in a $KI/I_2/H_2O$ (mass ratio 4:1:40) solution for 2 min, to remove (i) the gold catalyst used during the growth process, (ii) the native SiO_x, and (iii) possible gold contaminants on the Si NW surface. Following the initial pretreatment process, the Si NWs were dispersed in ethanol, using ultrasonication for 6 s. The dispersed Si NWs, probably because of the ultrasonic process, exhibited relatively higher length distribution (4−10 μm) than the Si NWs attached to growth batch (7−10 μm).

Si NWs dispersed in ethanol were deposited on a precleaned p-Si(100) (0.001 Ω cm resistivity) "receiver" substrate with 300 nm thermal oxide and a Ti/Au (10/200 nm) bottom gate electrode. The deposition method used in the current study is based on a spray-coating process under controlled conditions (Figure 1) that was

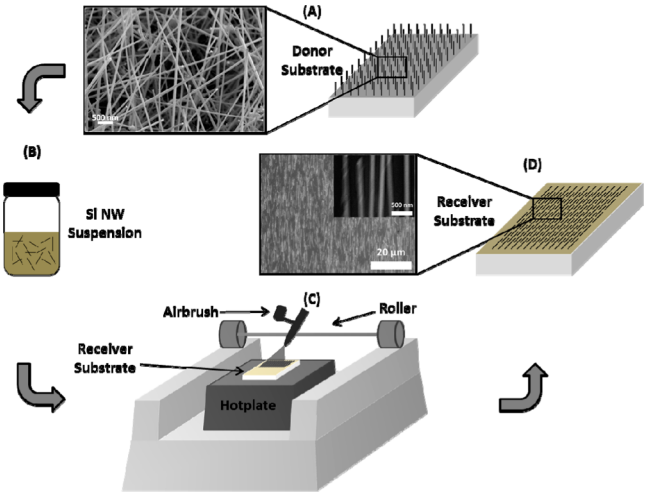


Figure 1. Schematics of the spray-coating process that involves a direct transfer of Si NW suspension to the receiver substrates. (A) Schematics and scanning electron microscopy image of the Si NWs sample used in this study. (B) Schematics of the Si NWs suspension. (C) Schematics of the assembled apparatus used in this study. (D) Schematics and scanning electron microscopy image of Si NW spray-coated on SiO_x/Si substrate. Reproduced with permission from ref 11. Copyright 2012 American Chemical Society.

reported elsewhere.[11] Briefly, the deposition of the Si NWs started with the placement of the "receiver" substrate on a hot plate at 75 °C.[11] The suspension of Si NWs was then applied using a spray gun (Prona R2-F) with 40 psi carrier gas (nitrogen) pressure and with a tilting angle of (5 ± 2)° relative to the "receiver" substrate. The nozzle tip was usually held at a distance of 1 cm from the substrate. Images of the Si NWs after the deposition were obtained using a scanning electron microscope (e-LiNE, Raith, Dortmund, Germany) and by an optical microscope (Olympus BX51RF-5) that is equipped with a camera (Olympus CAM-LC20-Bundle).[11]

Fabrication of Si NW Field-Effect Transistors. Prior to the device fabrication, the top substrate was cleaned by ultrasonic treatment in acetone, methanol, and ethanol and slightly etched using oxygen plasma (50 W; 1 min) for removing residues of organic contaminations. Eighteen pairs of 1300 μm long and 2 μm wide interdigitated Ti/Au (30/110 nm) source/drain (S/D) electrodes with an interelectrode spacing of 2 μm were defined on top of the sprayed Si NWs array using photolithography (Karl Suss MA6Mask Aligner). The native oxide at the edges of the Si NWs, which are supposed to be coated with metallic contacts, etched by buffered hydrofluoric acid for 5 s immediately before being loaded into the metal deposition system. The metal contacts were applied by conventional lift-off process. In a few cases, individual Si NWs were contacted with S/D Ti/Au (30/110 nm) electrodes with a channel length of 2 μm, using e-beam lithography and lift-off processes, as described elsewhere.[4−6] The number of bridged Si NWs between the S/D electrodes was evaluated by an optical microscope (Olympus BX51RF-5) in dark field mode and scanning electron microscope (e-LiNE, Raith, Dortmund, Germany).[11]

Electrical Characterization of Si NW Field-Effect Transistors. An Agilent B1500A Semiconductor device analyzer was used for the electrical measurements. To assess the electrical characteristics of the *aa*-Si NW FETs and of the individual Si NW FETs (*i*-Si NW FETs), S/D current (I_{ds}) versus voltage dependent back-gate (V_g) measurements, swept backward between +40 V to −40 V with 200 mV steps and at 2 V S/D voltage (V_{ds}), were carried out under ambient conditions.

High-Resolution Transmission Electron Microscopy. Following the electrical characterization, selected *aa*-Si NW FETs and *i*-Si NW FETs were etched in buffered hydrofluoric acid for 15 s and in a $KI/I_2/H_2O$ (mass ratio 4:1:40) solution for 2 min, to remove the SiO_x as well potential Au impurities from the Si NW surface. At the end of the etching process, the Si NWs were ultrasonically detached from the FET device and transferred, via an interfacing ethanol drop, to TEM copper grids. High-resolution transmission electron microscopy (HRTEM; FEI Titan 80−300 keV S/TEM operating at 300 keV) and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) were then carried out to analyze the surface and structure of the detached Si NWs.

RESULTS

Preparation of Si NW Arrays. Figure 2 shows representative optical (dark field) microscopy images of spray-coated Si NWs on a SiO_x/Si substrate at optimal gas pressure (40 psi). As seen in the figure, more than 90% of the Si NWs were aligned within ±10° of the main flow direction. The rest of the Si NWs were distributed between ca. −30° to +30° with respect to the flow direction.[11] The density of the aligned Si NWs was controlled by the spray coating time.[11] The higher the spray-coating time the higher the density of the deposited Si NWs. For example, 5 s flow duration produced Si NW arrays with an average NW-NW separation of ∼8 μm (see Figure 2a). A 20 s deposition time produced Si NW arrays with an average NW-NW separation of ∼2 μm (see Figure 2b). Extended deposition time (∼30 s) produced Si NW arrays with (reduced) average NW-NW separation of ∼1 μm (see Figure 2c).

The high alignment of the Si NW arrays can be attributed mainly to the dynamics of the droplet formation during the spray-coating process, which can be understood by a combined action of viscous shear forces and capillary forces.[11] Provided that the size of the deposited droplet, which can be controlled by the nozzle size of the spray gun, is comparable with the length of the single Si NW, the shear-driven elongation of the generated droplets results presumably in the alignment of the confined Si NWs in the spraying direction. Flattening and possibly inertial elongation in the spraying direction of the micro droplets upon their impact onto the substrate yields fast immobilization of the aligned Si NWs on the surface due to van der Waals attraction. Having the substrate at a temperature that is close to the boiling point of the suspension's solvent (ethanol; $T_{boiling} \approx 74.4$ °C) enhances solvent evaporation, yielding thinner solvent films and better interaction between the Si NWs and the substrate upon impact.[11]

Figure 3 presents scanning electron microscopy images of a representative *aa*-Si NWs that are contacted with interdigitated S/D electrodes. As could be seen, the contacted Si NWs are aligned parallel to each other (within ±10° deviation) and no

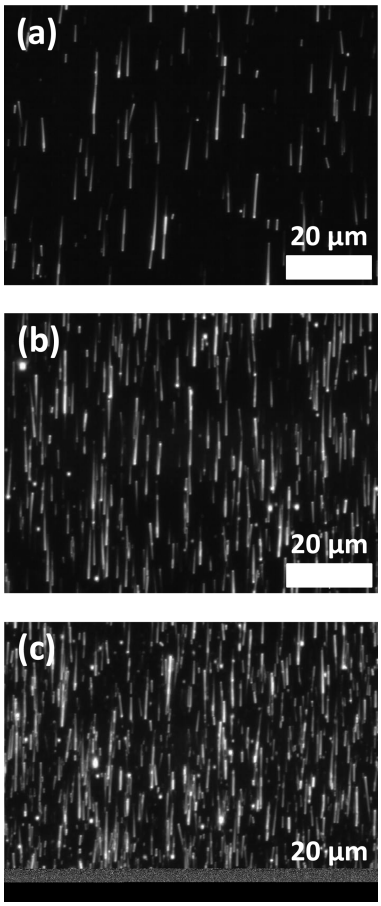


Figure 2. Optical microscopy (dark field) images of Si NWs aligned by spray flow for different durations: (a) 5 s; (b) 20 s; and (c) 30 s. All experiments were carried out with an air pressure of 40 psi at a substrate temperature of 75 °C.

Figure 3. Scanning electron microscopy images of representative *aa*-Si NW FET: (a) a low magnification of the device; (b) a high magnification of the selected area in panel ″a″, where three types of contacted Si NWs are highlighted: (i) contacted Si NW with one edge beneath the source electrode and the opposite edge beneath the drain electrode; (ii) contacted Si NW with both edges in the subsequent nonmetallized gaps; and (iii) Si NW with one edge contacted by one electrode and with the opposite edge located in the gap between the adjacent S/D electrodes; and (c) a high magnification of the selected area in panel b.

overlap between adjacent Si NWs is observed (Figure 3b). One part of the Si NWs is contacted with one edge beneath the source electrode and the opposite edge beneath the drain electrode (Figure 3b(i) and c). The second part of the Si NWs is contacted by two adjacent electrodes, but with (one or both) edges in the subsequent nonmetallized gaps. The third part of the Si NWs is contacted by one electrode from one side, but with the opposite edge located in the gap between the adjacent S/D electrodes. Under the experimental conditions of the current study, it is reasonable to assume that the electrical contributions of the first and second parts of the contacted Si NWs are similar to each other. Additionally, it is reasonable to assume that the third part of contacted Si NWs does not contribute to the overall device performance.

Electrical Characterization of the *aa*-Si NW FETs. Figure 4a shows typical output characteristics of *aa*-Si NW FET with 60 Si NWs between S/D electrodes at room temperature. As seen in the figure, the $I_{ds}-V_{ds}$ curves near the V_{ds} = 0 V regime exhibit almost linear behavior, indicating that the electrical contact between the metal electrodes and the aa-Si NWs is Ohmic.[23] Statistical analysis has shown that the electrical contacts between the metal electrodes and Si NWs in all studied devices are almost the same. Therefore, any differences between the examined devices shall be ascribed to the intrinsic properties of the Si NWs per se. Figure 4b summarizes the FET transfer characteristics of the 60 conducting Si NWs between the S/D electrodes. As seen in the figure, the I_{ds} versus V_{ds} behavior exhibit a typical accumulation mode of p-channel transistor behavior. At V_{ds} = 2 V, the on-current (I_{on}), viz. the I_{ds} at V_g = +40 V, is 19.86 μA; the off-current (I_{off}), viz. the I_{ds} at V_g = −40 V, is 0.54 nA; and the I_{on}/I_{off} is 3.7 × 10^4. The linear regime of the transconductance (g_m) is ∼0.8 μS and the threshold voltage (V_{th}) is ∼10.2 V.

To study the effect of the bridged Si NWs on the *aa*-Si NW FET performance, we have fabricated and measured 87 FET devices with varied number of Si NWs on similar interdigitated electrodes. The number of bridged Si NWs in each FET device, *n*, was determined via optical microscopy. Figure 5 presents the measured electrical signals (I_{on}, I_{off}, and I_{on}/I_{off}) as a function of *n*. As seen in the figure, the I_{on} increases almost linearly with *n*, with relatively high variance at $n < 80$ and relatively low variance at $n > 80$. This trend is consistent with previous findings on aligned carbon nanotubes[32,33] as well as Si NWs.[34] Unlike the I_{on}, the I_{off} shows random distribution at $3 \leq n < 80$ (Figure 5b). For $n > 80$, the I_{off} shows a trend with a positive slope. The I_{on}/I_{off} shows random distribution in the region of $3 \leq n < 80$, with values ranging between 1×10^1 to 1×10^7 (Figure 5c). In this region, 83% of the devices exhibit $I_{on}/I_{off} > 1 \times 10^2$, while the rest exhibit $I_{on}/I_{off} < 1 \times 10^2$. For $n > 80$, the I_{on}/I_{off} ratio exhibits a trend that converges to a fixed level. In this region, 35% of the devices exhibit $I_{on}/I_{off} > 1 \times 10^2$ and the rest (65%) of the devices exhibit $I_{on}/I_{off} < 1 \times 10^2$. Only one device with $I_{on}/I_{off} > 1 \times 10^3$ was obtained in the region of $n > 80$. Normalizing the on-state conductance ($\overline{G}_{on}$) and the off-state conductance ($\overline{G}_{off}$) of each device by the related number of Si NWs (Figure 5d) shows that $\overline{G}_{on}$ is distributed in a narrow interval (1×10^{-8} to 1×10^{-6} S) for $3 \leq n < 30$ and in a narrower interval for $n > 30$. For the latter, $\overline{G}_{on}$ approaches a constant value of 3×10^{-7} S. $\overline{G}_{off}$ shows larger scattering than $\overline{G}_{on}$ and varies in a wide interval (1×10^{-13} to 1×10^{-8} S) for $3 < n < 80$ and in a narrow interval (1×10^{-9} to 1×10^{-7} S) for $n > 80$. Because the current is proportional to the conductance at a given V_{ds}, it can be inferred that $I_{on}/I_{off} = \overline{G}_{on}/\overline{G}_{off}$. Although *aa*-Si NW FET with $n > 80$ exhibit more uniform device parameters than *aa*-Si NW FETs with $3 \leq n < 80$, the obtained

Figure 4. (a) I_{ds} versus V_{ds} plots of a FET device with 60 bridged Si NWs at V_g = +40 V, +30 V, +20 V, +10 V, 0 V, −10 V, −20 V, −30 V, and −40 V from bottom to up. Inset: I_{ds} versus V_{ds} curves near V_{ds} = 0 V. (b) Linear scale (black line; left axis) and log scale (blue line; right axis) plots of I_{ds} versus V_g at V_{ds} = 2 V.

Figure 5. (a) I_{on} as a function of n; (b) I_{off} as a function of n; (c) I_{on}/I_{off} ratio as a function of n; and (d) $\overline{G}_{on}$ and $\overline{G}_{off}$ as a function of n. All measurements were performed with V_g sweeping from +40 to −40 V and with V_{ds} = 2 V.

parameters might not be appropriate for practical or efficient "switching" applications.

Apart from the effect of the Si NW number on I_{on}, I_{off}, and I_{on}/I_{off}, we also studied the scaling effect of g_m, hole mobility (μ_h) and V_{th}. As seen in Figure 6a, g_m increases almost linearly with n, implying for an additive behavior. The μ_h of a single Si NW in *aa*-Si NW FETs can be calculated using the following relationship[34]

$$\mu_h = \frac{g_m \ln[(2t_{ox} + R_{NW})/R_{NW}]}{2\pi\varepsilon_{ox} n} \frac{L_{NW}}{V_{ds}} \quad (1)$$

where t_{ox} is the thickness of the gate oxide, ε_{ox} is the dielectric permittivity of the oxide, R_{NW} is the radius of the Si NW, and L_{NW} is the length of the channel. The results are presented in Figure 6b. As seen in the figure, the data points are distributed in an interval of ∼0.7 to ∼6.3 $cm^2/V{\cdot}s$. The distribution of the data points becomes narrower as n increases. The V_{th} versus n plot (Figure 6c) shows a wide distribution (5−36 V) that is not affected by the n value. This could be attributed to hysteresis in the electrical characteristics of the *aa*-Si NW FET (not shown), probably due to surface states (such as dangling bonds, defects, and adsorbates) variances between one Si NW and another.[4−6,35]

DISCUSSION

Relation between Individual Si NWs and Si NW Arrays. It is likely that the conductance of *aa*-Si NW FETs is equal to the sum of the individual Si NW FETs (*i*-Si NW FETs) that are connected in parallel. To validate this hypothesis, we have fabricated 24 *i*-Si NW FETs (see Figure 7a) and measured their electrical characteristics. The results show that part of the *i*-Si NW FETs exhibits $I_{on}/I_{off} > 1 \times 10^2$

Figure 6. (a) g_m; (b) μ_h; and (c) V_{th} as a function of the bridged Si NW number, *n*.

(hereon, **Type-A** Si NWs; see Figure 7b), whereas the other part of the *i*-Si NW FETs exhibits $I_{on}/I_{off} < 1 \times 10^2$ (hereon, **Type-B** Si NWs; see Figure 7c). The output curves of all measured devices exhibit linearity near $V_{ds} = 0$ V, indicating that the electrical contacts between the metallic electrodes and Si NWs are Ohmic. Therefore, the different characteristics of the examined *i*-Si NW FETs shall be attributed to the intrinsic properties of the Si NWs per se.

Figure 8a presents a histogram of the logarithmic I_{on}/I_{off} values for the measured *i*-Si NW FETs. As shown in the figure, 83% of the *i*-Si NW FETs have Type-A characteristics and 17% of the *i*-Si NW FETs have Type-B characteristics. Figure 8b shows the distribution of the logarithmic values of G_{on}(*Log* G_{on}) and G_{off} (*Log* G_{off}) for the measured *i*-Si NW FETs. As seen in the figure, the *Log*G_{on} has a mean value (μ) of −6.63 and a standard deviation (σ) of 0.98. The *Log* G_{off} has a mean value of −10.6 and a standard deviation of 1.84.[36] This

Figure 7. (a) Scanning electron microscopy image of a representative *i*-Si NW FET and (b, c) linear scale (black lines; left axis) and log scale (blue lines; right axis) plots of I_{ds} versus V_g of representative (b) Type-A *i*-Si NW FET and (c) Type-B *i*-Si NW FET.

indicates that G_{off} and I_{off} exhibit higher device-to-device variations than G_{on} and I_{on}.

In the following, we discuss the electrical characteristics of the *aa*-Si NW FETs by means of *i*-Si NW FETs. This presentation can be described as a binomial sampling experiment.[37] For this purpose, we use p and $q = 1\text{-}p$ to denote the probability of fabricated *i*-Si NW FETs that are bridged with Type-A and Type-B Si NWs, respectively. Using these terms, the mean values of G_{off} and G_{on} of *i*-Si NW FETs, denoted by $\mu_{G_{off}}$ and $\mu_{G_{on}}$, are given by

$$\mu_{G_{off}} = pG_{off}^{A} + qG_{off}^{B} \quad (2)$$

$$\mu_{G_{on}} = pG_{on}^{A} + qG_{on}^{B} \quad (3)$$

dx.doi.org/10.1021/am300961d | *ACS Appl. Mater. Interfaces* 2012, 4, 4251−4258

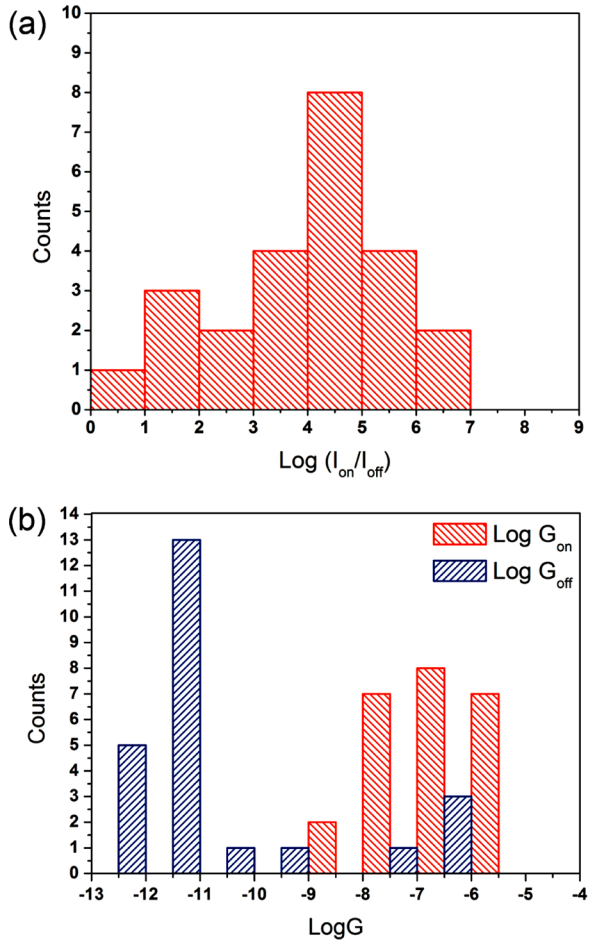


Figure 8. Histogram of the logarithmic values of the (a) I_{on}/I_{off} ratio, and (b) G_{off} and G_{on} for the measured *i*-Si NW FETs.

where G^{A}_{off} is the G_{off} of Type-A Si NW, G^{B}_{off} is the G_{off} of Type-B Si NW, G^{A}_{on} is the G_{on} of Type-A Si NW, and G^{B}_{on} is the G_{on} of Type-B Si NW. Let n denote the total number of conducting channels in the *aa*-Si NW FET and let k denote the number of channels that are bridged with Type-A Si NWs, where $k = 0, 1, 2, ..., n$. The probability that an arbitrary *aa*-Si NW FET device with n channels has Type-A Si NWs, denoted by $p(k)$, is given by

$$p(k) = \binom{n}{k} p^k q^{n-k} \tag{4}$$

where $\binom{n}{k}$ stands for the binomial coefficient. The expectation of G_{off} with n channels $E(G^{n}_{off})$, is computed as follows

$$E(G^{n}_{off}) \sum_{k=0}^{n} \binom{n}{k} p^k q^{n-k} [kG^{A}_{off} + (n-k)G^{B}_{off}]$$

$$= \sum_{k=0}^{n} \frac{n!}{k!(n-k)} p^k q^{n-k} [k(G^{A}_{off} - G^{B}_{off}) + nG^{B}_{off}]$$

$$= n\mu_{G_{off}} \tag{5}$$

Similarly, the expectation of G_{on} of n channels $E(G^{n}_{on})$, is computed as follows

$$E(G^{n}_{on}) = n\mu_{G_{on}} \tag{6}$$

Thus, the I_{on}/I_{off} ratio of the *aa*-Si NW FET is

$$\frac{I_{on}}{I_{off}} = \frac{E(G^{n}_{on})V_{ds}}{E(G^{n}_{off})V_{ds}} = \frac{\mu_{G_{on}}}{\mu_{G_{off}}} \tag{7}$$

For high n values, eqs 5−7 suggest that the G_{off} and G_{on} of *aa*-Si NW FETs increase linearly with the number of the bridged Si NWs and that the I_{on}/I_{off} ratio remains constant. Using typical characteristics of Type-A Si NWs ($G_{on} = 1 \times 10^{-7}$ S, $G_{off} = 1 \times 10^{-12}$ S, *and* $p = 0.9$) and Type-B Si NWs ($G_{on} = 10^{-7}$ S, $G_{off} = 1 \times 10^{-8}$ S and $q = 0.1$), eq 7 gives $I_{on}/I_{off} = 1 \times 10^{2}$ for $n > 80$. This suggests that the I_{on}/I_{off} ratio of *aa*-Si NW FETs with $n > 80$ is highly dependent on the fraction of Type-B Si NWs from the array. To get *aa*-Si NW FET with high I_{on}/I_{off} ratio in the $n > 80$ region, one should remove or decrease the concentration of Type-A Si NWs in the *aa*-Si NW FET. For the $3 \leq n < 80$ region, the random and highly distributed results indicate that Type-B Si NWs affect the electrical characteristics of the *aa*-Si NW FET, more than Type-B Si NWs.

Analysis of Individual Si NWs by High-Resolution Transmission Electron Microscopy. To gain a deeper insight into the differences between the examined Si NW FETs, we measured the Si NWs by high-resolution transmission electron microscopy (HRTEM) after they were detached from *i*-Si NW FET—see the Experimental Section. As seen in Figure 9a, Type-A Si NWs have single-crystalline structure that is free from metallic impurities. In contrast, Type-B Si NWs incorporate Au nanoparticles in the Si NWs (Figure 9b)—an observation that is further confirmed by HAADF-STEM and energy-dispersive X-ray spectroscopy (EDX) measurements (Figure 9c, d). The observation of Au nanoparticles before and after etching Type-B Si NWs with Au and SiO_x etchants (see Experimental Section) indicates that the Au impurities are located mostly inside the Si NW cores (cf. also refs 36 and 37). With this in mind, it is reasonable to argue that the Au nanoparticles act as carrier generation centers that increase the I_{off} of the related Si NW FETs (cf. Figure 7c).

SUMMARY AND CONCLUSIONS

A systematic scaling study shows that a small number of bridged Si NW channels ($3 \leq n < 80$) provide random electrical features in *aa*-Si NW FETs. High numbers of bridged Si NWs ($n > 80$) increases the I_{on} and I_{off} linearly with n, but remains the I_{on}/I_{off} ratio, μ_h and the V_{th} unaffected. These results are explained by the fact that *aa*-Si NWs contain two main groups of Si NWs: (i) a group of Si NWs with no gold impurities that exhibit high and uniform electrical characteristics ($I_{on}/I_{off} > 1 \times 10^{2}$; Type-A Si NW); and (ii) a group of Si NWs with gold impurities that exhibit inferior electrical characteristics ($I_{on}/I_{off} < 1 \times 10^{2}$; Type-B Si NW). Complementary binomial analysis indicates that the obtained discrepancies could be explained by a weighted contribution of such two main groups of Si NWs, which could exist in any Si NWs batch that is grown by chemical vapor deposition with gold catalyst or by similar catalyst-based growth techniques. These findings suggest that the uniform diameter, length and shape of a grown batch of Si NWs do not necessarily imply uniform electrical characteristics. Advanced growth processes of (electrically) homogeneous Si NWs[39] and/or advanced sorting techniques[40,41] (cf. also ref 42 for self-sorting of carbon nanotubes) are therefore of critical importance for bringing the *aa*-Si NWs device concept to a reliable technological phase.

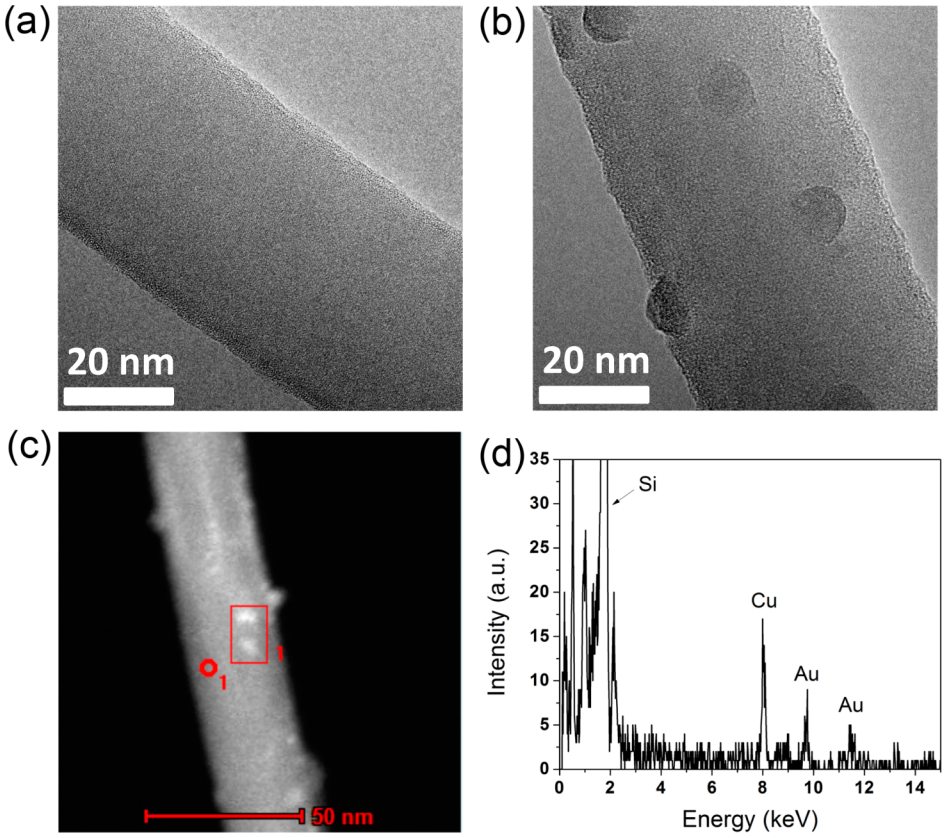


Figure 9. HRTEM image of a typical (a) Type-A Si NW and (b) Type-B Si NW. (c) HADDF-STEM image and (d) EDX spectra of Au nanoparticles in a Type-B Si NW.

AUTHOR INFORMATION

Corresponding Author

*E-mail: hhossam@technion.ac.il.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The research leading to these results has received funding from the FP7-Health Program under the LCAOS (grant agreement 258868). The authors acknowledge Dr. Yair Paska for fruitful discussions and Dr. Mirjam (Ulrike) Tisch, for reviewing the manuscript. H.H. is a Knight of the Order of Academic Palms.

REFERENCES

(1) Barth, S.; Hernandez-Ramirez, F.; Holmes, J. D.; Romano-Rodriguez, A. *Prog. Mater. Sci.* **2010**, *55*, 563−627.

(2) Tisch, U.; Haick, H. *MRS Bull.* **2010**, *35*, 797−803.

(3) Bashouti, M. Y.; Tung, R. T.; Haick, H. *Small* **2009**, *5*, 2761−2769.

(4) Paska, Y.; Stelzner, T.; Assad, O.; Tisch, U.; Christiansen, S.; Haick, H. *ACS Nano* **2012**, *6*, 335−345.

(5) Paska, Y.; Stelzner, T.; Christiansen, S.; Haick, H. *ACS Nano* **2011**, *5*, 5620−5626.

(6) Paska, Y.; Haick, H. *ACS Appl. Mater. Interfaves* **2012**, *4*, 2604−2617.

(7) Huang, Z.; Wang, R.; Jia, D.; Maoying, L.; Humphrey, M. G.; Zhang, C. *ACS Appl. Mater. Interfaces* **2012**, *4*, 1553−1559.

(8) Wei, L.; Ping, X.; Lieber, C. M. *IEEE Electron Device Lett.* **2008**, *55*, 2859−2876.

(9) Chau, R.; Doyle, B.; Datta, S.; Kavalieros, J.; Zhang, K. *Nat. Mater.* **2007**, *6*, 810−812.

(10) Masood, M. N.; Chen, S.; Carlen, E. T.; van den Berg, A. *ACS Appl. Mater. Interfaces* **2010**, *2*, 3422−3428.

(11) Assad, O.; Leshansky, A. M.; Wang, B.; Stelzner, T.; Christiansen, S.; Haick, H. *ACS Nano* **2012**, *6*, 4702−4712.

(12) Wong, W. S.; Raychaudhuri, S.; Lujan, R.; Sambandan, S.; Street, R. A. *Nano Lett.* **2011**, *11*, 2214−2218.

(13) Street, R. A. *Adv. Mater.* **2009**, *21*, 2007−2022.

(14) Pui, T.-S.; Agarwal, A.; Ye, F.; Balasubramanian, N.; Chen, P. *Small* **2009**, *5*, 208−212.

(15) Stern, E.; Vacic, A.; Reed, M. A. *IEEE Trans. Electron Devices* **2008**, *55*, 3119−3130.

(16) McAlpine, M. C.; Ahmad, H.; Wang, D. W.; Heath, J. R. *Nat. Mater.* **2007**, *6*, 379−384.

(17) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. *Nano Lett.* **2006**, *6*, 973−977.

(18) Duan, X. F.; Niu, C. M.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. L. *Nature* **2003**, *425*, 274−278.

(19) Fan, Z. Y.; Ho, J. C.; Jacobson, Z. A.; Razavi, H.; Javey, A. *Proc. Nat. Acad. Sci. U.S.A.* **2008**, *105*, 11066−11070.

(20) Fan, Z.; Ho, J. C.; Takahashi, T.; Yerushalmi, R.; Takei, K.; Ford, A. A.; Chueh, Y.-L.; Javey, A. *Adv. Mater.* **2009**, *21*, 3730−3743.

(21) Gunawan, O.; Sekaric, L.; Majumdar, A.; Rooks, M.; Appenzeller, J.; Sleight, J.; Guha, S.; Haensch, W. *Nano Lett.* **2008**, *8*, 1566−1571.

(22) Wang, M. C. P.; Gates, B. D. *Mater. Today* **2009**, *12*, 34−43.

(23) Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem. B* **2000**, *104*, 5213−5216.

(24) Ford, A. C.; Ho, J. C.; Chueh, Y.-L.; Tseng, Y.-C.; Fan, Z.; Guo, J.; Bokor, J.; Javey, A. *Nano Lett.* **2008**, *9*, 360−365.

(25) Black, C. T. *Appl. Phys. Lett.* **2005**, *87*, 1631161−3.

(26) Zhang, D.; Liu, Z.; Li, C.; Tang, T.; Liu, X.; Han, S.; Lei, B.; Zhou, C. *Nano Lett.* **2004**, *4*, 1919−1924.

(27) Fan, Z.; Lu, J. G. *IEEE Trans. Nanotechnol.* **2006**, *5*, 393−396.

(28) Stern, E.; Klemic, J. F.; Routenberg, D. A.; Wyrembak, P. N.; Turner-Evans, D. B.; Hamilton, A. D.; LaVan, D. A.; Fahmy, T. M.; Reed, M. A. *Nature* **2007**, *445*, 519−522.
(29) Li, J.; Zhang, Y.; To, S.; You, L.; Sun, Y. *ACS Nano* **2011**, *5*, 6661−6668.
(30) Elfstrom, N.; Juhasz, R.; Sychugov, I.; Engfeldt, T.; Karlstrom, A. E.; Linnros, J. *Nano Lett.* **2007**, *7* (9), 2608−2612.
(31) Stelzner, T.; Andrä, G.; Wendler, E.; Wesch, W.; Scholz, R.; Gösele, U.; Christiansen, S. *Nanotechnology* **2006**, *17*, 2895−2898.
(32) Kang, S. J.; Kocabas, C.; Ozel, T.; Shim, M.; Pimparkar, N.; Alam, M. A.; Rotkin, S. V.; Rogers, J. A. *Nat. Nanotechol.* **2007**, *2*, 230−236.
(33) Franklin, A. D.; Wong, H. S. P.; Lin, A.; Chen, Z. H. *IEEE Electron Device Lett.* **2010**, *31*, 644−646.
(34) Fan, Z.; Ho, J. C.; Jacobson, Z. A.; Yerushalmi, R.; Alley, R. L.; Razavi, H.; Javey, A. *Nano Lett.* **2007**, *8* (1), 20−25.
(35) Jie, J.; Zhang, W.; Peng, K.; Yuan, G.; Lee, C. S.; Lee, S.-T. *Adv. Funct. Mater.* **2008**, *18*, 3251−3257.
(36) Due to the small standard deviations in the log G_{on}, it is difficult to use the G_{on} for identifying the device-to-device variations for Type-A and Type-B Si NW FETs. Rather, Type-A and Type-B Si NW FETs can be identified by G_{off}.
(37) Lipschutz, S.; Schiller, J. *Introduction to Probability and Statistics*; McGraw-Hill: New York, 1998; Vol. *7*.
(38) Sprokel, G. J.; Fairfield, J. M. *J. Electrochem. Soc.* **1965**, *112*, 200−203.
(39) Mikhael, B.; Elise, B.; Xavier, M.; Sebastian, S.; Johann, M.; Laetitia, P. *ACS Appl. Mater. Interfaces* **2011**, *3*, 3866−3873.
(40) Perea, D. E.; Hemesath, E. R.; Schwalbach, E. J.; Lensch-Falk, J. L.; Voorhees, P. W.; Lauhon, L. G. *Nat. Nanotechnol.* **2009**, *4*, 315−319.
(41) Koren, E.; Berkovitch, N.; Rosenwaks, Y. *Nano Lett.* **2010**, *10*, 1163−1167.
(42) LeMieux, M. C.; Roberts, M.; Barman, S.; Jin, Y. W.; Kim, J. M.; Bao, Z. *Science* **2008**, *321*, 101−104.